Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A voltage level shifter comprising:

a front stage circuit periodically generating a pair of non-complementary control signals including a first control signal and a second control signal having different maximum voltage levels in response to a first input clock signal and a second input clock signal complementary to said first input clock signal;

a switch circuit including two PMOS transistors connected between a maximum voltage and a minimum voltage in series, wherein a third control signal is outputted from a conjunction of said two PMOS transistors, and said first and second control signals are coupled to the gate electrodes of said two PMOS transistors, respectively; and

a driving circuit receiving said third control signal and outputting an output clock signal.

2. (Original) The voltage level shifter according to claim 1 wherein said front stage circuit includes:

a first PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said first input clock signal, and the source electrode serving as an output end of said first control signal;

a second PMOS transistor having the gate electrode serving as an output end of said second control signal, the drain electrode coupled to said output end of said first control signal and the source electrode coupled to said maximum voltage;

a third PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said second input clock signal, and the source electrode coupled to said output end of said second control signal; and

a fourth PMOS transistor having the gate electrode coupled to said first input clock signal, the drain electrode coupled to said output end of said second control signal and the source electrode coupled to said maximum voltage.

3. (Original) The voltage level shifter according to claim 1 wherein said driving circuit includes:

a fifth PMOS transistor having the gate electrode coupled to said third control signal, the source electrode coupled to said maximum voltage and the drain electrode serving as a voltage node;

a sixth PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said minimum voltage and the source electrode coupled to said voltage node;

a seventh PMOS transistor having the gate electrode coupled to said voltage node, the source electrode coupled to said output end of said output clock signal and the drain electrode coupled to said minimum voltage; and

an eighth PMOS transistor having the gate electrode coupled to said third control signal, the drain electrode coupled to said output end of said output clock signal, and the source electrode coupled to said maximum voltage.

4. (Original) The voltage level shifter according to claim 1 wherein said output clock signal has a peak-to-peak value larger than a peak-to-peak value of said input clock signal.

5. (Original) A voltage level shifter comprising:

a first PMOS transistor having the gate electrode and the drain electrode connected to each other and further coupled to an input clock signal and the source electrode serving as an output end of a first control signal;

a second PMOS transistor having the gate electrode serving as an output end of a second control signal, the drain electrode coupled to said output end of said first control signal and the source electrode coupled to a maximum voltage;

a third PMOS transistor having the gate electrode and the drain electrode connected to each other and further coupled to a complementary signal relative to said input clock signal, the source electrode coupled to said output end of said second control signal;

a fourth PMOS transistor having the gate electrode coupled to said input clock signal, the drain electrode coupled to said output end of said second control signal and the source electrode coupled to said maximum voltage;

a switch circuit periodically generating a third control signal in response to said first and second control signals; and

a driving circuit receiving said third control signal and outputting an output clock signal having a peak-to-peak value larger than a peak-to-peak value of said input clock signal.

6. (Original) The voltage level shifter according to claim 5 wherein said switch circuit includes:

a fifth PMOS transistor having the gate electrode coupled to said first control signal, the drain electrode coupled to a minimum voltage and the source electrode serving as an output end of said third control signal; and

a sixth PMOS transistor having the gate electrode coupled to said second control signal, the drain electrode coupled said output end of said third control signal and the source electrode coupled to said maximum voltage.

7. (Original) The voltage level shifter according to claim 5 wherein said driving circuit includes:

a seventh PMOS transistor having the gate electrode coupled to said third control signal, the source electrode coupled to said maximum voltage and the drain electrode serving as a voltage node;

an eighth PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said minimum voltage and the source electrode coupled to said voltage node;

a ninth PMOS transistor having the gate electrode coupled to said voltage node, the source electrode coupled to said output end of said output clock signal and the drain electrode coupled to said minimum voltage; and

a tenth PMOS transistor having the gate electrode coupled to said third control signal, the drain electrode coupled to said output end of said output clock signal, and the source electrode coupled to said maximum voltage.

8. (Currently Amended) A voltage level shifter for converting an input clock signal into an output clock signal, comprising:

a front stage circuit periodically generating a first control signal and a second control signal in response to said input clock signal and a complementary clock signal relative to said input clock signal;

a switch circuit periodically generating a third control signal in response to said first and second control signals;

a first PMOS transistor having the gate electrode coupled to said third control signal, the source electrode coupled to a maximum voltage and the drain electrode serving as a voltage node;

a second PMOS transistor having the gate and drain electrodes connected to each other and further coupled to a minimum voltage and the source electrode coupled to said voltage node;

a third PMOS transistor having the gate electrode coupled to said voltage node, the source electrode coupled to an output end of said output clock signal and the drain electrode coupled to said minimum voltage; and

a fourth PMOS transistor having the gate electrode coupled to said third control signal, the drain electrode coupled to said output end of said output clock signal, and the source electrode coupled to said maximum voltage.

9. (Original) The voltage level shifter according to claim 8 wherein said front stage circuit includes:

a fifth PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said input clock signal, and the source electrode serving as an output end of said first control signal;

a sixth PMOS transistor having the gate electrode serving as an output end of said second control signal, the drain electrode coupled to said output end of said first control signal and the source electrode coupled to said maximum voltage;

a seventh PMOS transistor having the gate and drain electrodes connected to each other and further coupled to said complementary clock signal, and the source electrode coupled to said output end of said second control signal;

an eighth PMOS transistor having the gate electrode coupled to said input clock signal, the drain electrode coupled to said output end of said second control signal and the source electrode coupled to said maximum voltage.

10. (Original) The voltage level shifter according to claim 8 wherein said switch circuit includes:

a ninth PMOS transistor having the gate electrode coupled to said first control signal, the drain electrode coupled to said minimum voltage and the source electrode serving as an output end of said third control signal; and

a tenth PMOS transistor having the gate electrode coupled to said second control signal, the drain electrode coupled said output end of said third control signal and the source electrode coupled to said maximum voltage.